STMicroelectronics
ADG - ASD & IPAD™ Division[1]
BU Protection

(1) ADG: Automotive and Discretes Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PCN
Product/Process Change Notification

Protection devices housed in SOT666 and SOT665 packages assembly transfer from current subco in Malaysia to another subco in China

Notification number:	ADG-DIS/18/10897	**Issue Date**	08/06/2018
Issued by	Aline Augis		
Product series affected by the change		SOT66x devices	
Type of change		Back end realization	

Description of the change

Change assembly and test site from the current subco in Malaysia to a subco located in China for protection devices housed in SOT666 and SOT665 packages.

Reason for change

The current assembly line will be terminated in December 2018.

Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade ("halogen-free").

Disposition of former products

Deliveries of former products will continue as long as stock last.

Marking and traceability

The traceability is ensured by the marking, by a new internal codification and the QA number.

Marking value is the same with 90° rotation for the new subco.
See below an example of the marking rotation.

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Current subco (Malaysia)	New subco (China)

Qualification complete date	Week 17 - 2018

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection	SOT665	**ESDALC6V1P5**	Available
	SOT666	**ESDA25-4BP6**	Available
		USBLC6-2P6	Week 21 - 2018

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
ESDALC6V1P5	Week 29-2018	Week 35-2018
ESDA14V2BP6		
ESDA25-4BP6		
ESDALC6V1-5P6		
USBLC6-2P6		

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	QRP18024 Attached

Reliability Evaluation Report

Qualification of new subcontractor for protection devices in SOT665 and SOT666 packages

General Information	
Product Description	*Protection*
Part Numbers	*ESDALC6V1P5* *ESDA14V2BP6* *ESDA25-4BP6* *ESDALC6V1-5P6* *ESDALC6V1-5P6M* *USBLC6-2P6*
Product Group	*ADG*
Product division	*ASD&IPAD*
Package	*SOT665, SOT666*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS FRANCE* *ST AMK SINGAPORE*
Assembly plant	*SUBCONTRACTOR - CHINA (9955)*
Reliability Lab	*ST TOURS FRANCE*

Reliability Assessment
PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1	04/04/2018	6	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY 5
5.1 TEST VEHICLES 5
5.2 TEST PLAN AND RESULTS SUMMARY 5
6 ANNEXES 6
6.1 TESTS DESCRIPTION 6

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
PC	Pre-conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
PCT / AC	Pressure Pot 2 bars / Autoclave
THB	Thermal Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test
IOLT / TF	Intermittent Operational Life Test / Thermal Fatigue
DPA	Destructive Physical Analysis
RSH	Resistance to Solder Heat
SD	Solderability

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim of this report is to qualify new assembly subcontractor for protection devices housed in SOT665 and SOT666 packages.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to product datasheets

4.2 Construction note

	USBLC6-2P6
Wafer/Die fab. information	
Wafer fab manufacturing location	ST AMK SINGAPORE
Technology / Process family	ASD-TRANSIL
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST AMK SINGAPORE
Assembly information	
Assembly site	SUBCONTRACTOR - CHINA
Package description	SOT 666
Final testing information	
Testing location	SUBCONTRACTOR - CHINA

	ESDALC6V1P5
Wafer/Die fab. information	
Wafer fab manufacturing location	TOURS-FRANCE
Technology / Process family	ASD-TRANSIL
Wafer Testing (EWS) information	
Electrical testing manufacturing location	TOURS-FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR - CHINA
Package description	SOT 665
Final testing information	
Testing location	SUBCONTRACTOR - CHINA

	ESDA25-4BP6, ESDA14V2BP6, ESDALC6V1-5P6
Wafer/Die fab. information	
Wafer fab manufacturing location	TOURS- FRANCE
Technology / Process family	ASD-TRANSIL
Wafer Testing (EWS) information	
Electrical testing manufacturing location	TOURS-FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR - CHINA
Package description	SOT 666
Final testing information	
Testing location	SUBCONTRACTOR - CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Die manufacturing	Assembly plant	Package	Comments
Lot 1	ESDA25-4BP6	ST TOURS	Subcontractor China	SOT 666	Qualification lots
Lot 2	ESDALC6V1P5			SOT 665	
Lot 3	ESDALCL6-4P6A	ST AMK		SOT 666	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						Lot 1	Lot 2	Lot 3
Die Oriented Tests								
HTRB	N	JESD22 A-108	Junction Temperature=150°C Tension=3V	153	504h		0/77	0/76
					1000h		0/77	0/76
HTRB	N	JESD22 A-108	Junction Temperature=150°C Tension=24V	77	504h	0/77		
					1000h	0/77		
Package Oriented Tests								
TC	Y	JESD22 A-104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)= -65°C	75	500cy	0/25	0/25	0/25
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=3V	48	168h		0/24	0/24
					504h		0/24	0/24
					1000h		0/24	0/24
THB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Tension=24V	24	168h	0/24		
					504h	0/24		
					1000h	0/24		

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS
						Lot 1
Package Oriented Tests						
DBT	N	DM 00112629	Fluxing followed by IR reflow	30	Visual inspection	0/30
Solderability	N	JESD22 B-102	Steam Ageing SnAgCu bath 245°C	10	Visual inspection	0/10
			Steam Ageing SnPb 220°C	10	Visual inspection	0/10
			Dry Ageing SnAgCu 245°C	10	Visual inspection	0/10
			Dry Ageing SnPb 220°C	10	Visual inspection	0/10

6 ANNEXES

6.1 Tests Description

Test name	Standard Reference	Description	Purpose
Die Oriented			
HTRB High Temperature Reverse Bias	JESD22 A-108	HTRB : High Temperature Reverse Bias HTFB / HTGB : High Temperature Forward (Gate) Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation; - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented			
TC Temperature Cycling	JESD22 A-104	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere..	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	JESD22 A-101	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Solderability	J-STD-002	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT Dead Bug Test	DM00112629	To evaluate the wettability of the SMD. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.